

### Introduction

The 1588 “industrial” Ethernet standard allows synchronization of time events across multiple devices connected on a single Ethernet network. A key design component of such synchronization is a time stamping module designed to add time information to Ethernet packets.

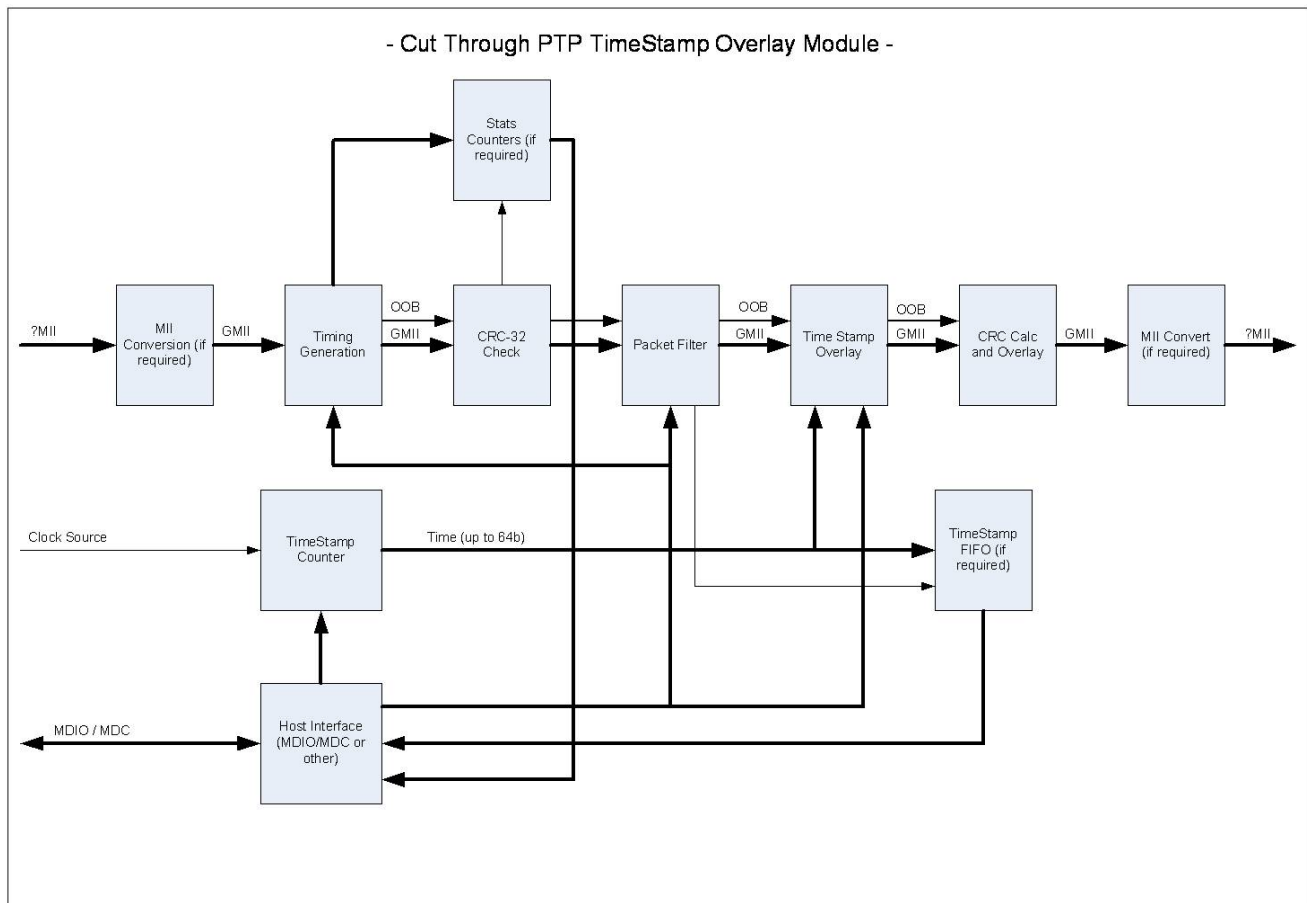
Octera provides such a time stamping design as a customizable module for Altera FPGAs. The design can be implemented with on-chip Serdes (Arria and Stratix families) or an external PHY for a low cost (Cyclone) FPGA design. The design can be licensed as source code and Octera offers customization under a design services engagement. The module can be combined with Octera’s verification environment (OCT-VER) to quickly develop an

FPGA implementing the 1588 time stamping functionality.

The IP consists of multiple modules not all of which are required depending on the features of the specific design.

### Features

- Fixed latency cut-through design.
- Packets are never de-framed and re-framed, hence IPGs are preserved.
- Requires an upstream MAC.
- Timer may be asynchronous to data path.
- Can support different media independent interfaces.
- Can support different host interfaces.
- Can support different time stamp sizes.
- Can support follow-on time stamping.



### **Implementation Summary**

<b>Core Specifics</b>		
Cyclone 3C5 and larger devices		
<b>Speed Grade</b>		
C8 or faster		
<b>Resource Utilization</b>		
	<i>Typical</i>	
LEs	3435	
Registers	2502	
RAM	33116	
<b>Supported Design Tools</b>		
Altera	Quartus II 9.0 or later	

### **Customization**

The design is offered with multiple optional modules to allow for a high level of customization in order to satisfy specific customer requirements. Please contact us to discuss your specific needs.

Examples of optional modules include:

- Interface modules to convert non-GMII to GMII.
- Timestamp FIFO to generate a follow on packet implementation.
- Avalon host bus interface defaults to MDIO / MDC however other protocols can be supported.

### **Deliverables**

- Verilog source code or encrypted source code depending upon license.
- Scripted verification environment including Ethernet traffic.
- Optional networking verification suite (OCT-VER) available.

**Product code: OCT-1588**