

### Introduction

DDR3 is the system memory of choice in high volume applications and is therefore the memory standard with the best availability, cost per density and longevity.

Standard DDR3 controllers normally operate at 300MHz and above, which is a higher I/O frequency than is available in low cost FPGAs. Octera's DDR3 controller uses the JEDEC standard DLL Disable mode of operation to operate the interface at 125MHz and is thus available for the low cost Altera Cyclone III and IV families.

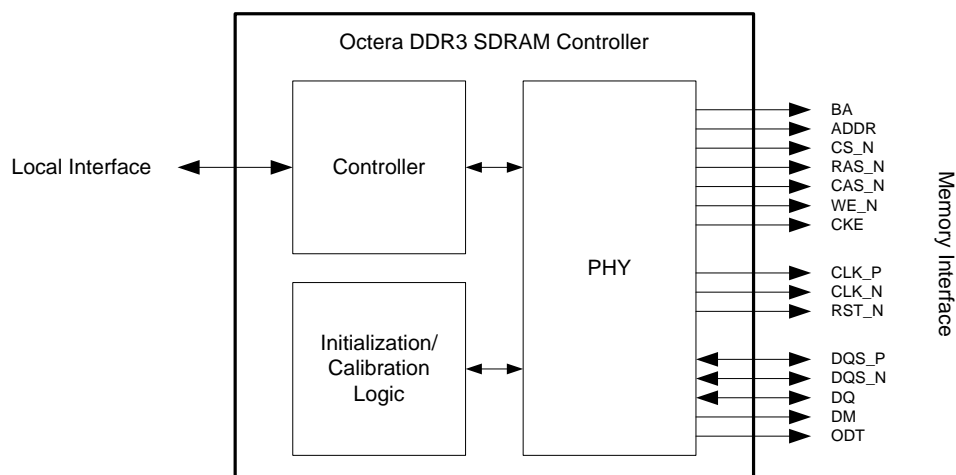
### Features

- Variable memory configuration (x4, x8, x16)
- Variable memory burst length
- Supports registered and unregistered DIMMs
- Selectable precharge address bit (8 or 10)

- Programmable mode register values
- Variable number of clock outputs
- Variable number of chip select outputs
- Variable number of clock enable outputs
- Variable number of bank address outputs
- Variable number of address outputs
- Variable number of data bits
- Variable number of data strobe bits
- Variable number of data mask bits

Compared to a standard DDR3 controller, Octera's controller has been designed to allow mode register writes and self-refresh commands prior to the completion of the initialization and calibration sequence. The calibration logic has also been modified to account for the wide read latency range specified when running in DLL Disable mode.

Also available is a version of the controller that preserves data present in memory that resides in the training area needed for calibration that would otherwise be overwritten.



**Implementation Summary**

<b>Core Specifics</b>		
Cyclone III, Cyclone IV		
<b>Speed Grade</b>		
All		
<b>Resource Utilization</b>		
	<i>Cyclone III</i>	<i>Cyclone IV</i>
LEs	3021	2917
Registers	1680	1623
RAM	3 x M9K	3 x M9K
<b>Supported Design Tools</b>		
Altera	Quartus II 9.1SP2 or later	

**Deliverables**

- Encrypted source code
- Scripted verification environment
- DDR3 Bus Functional Models

**Product codes:**  
**OCT-DDR3, OCT-DDR3-TADR**