

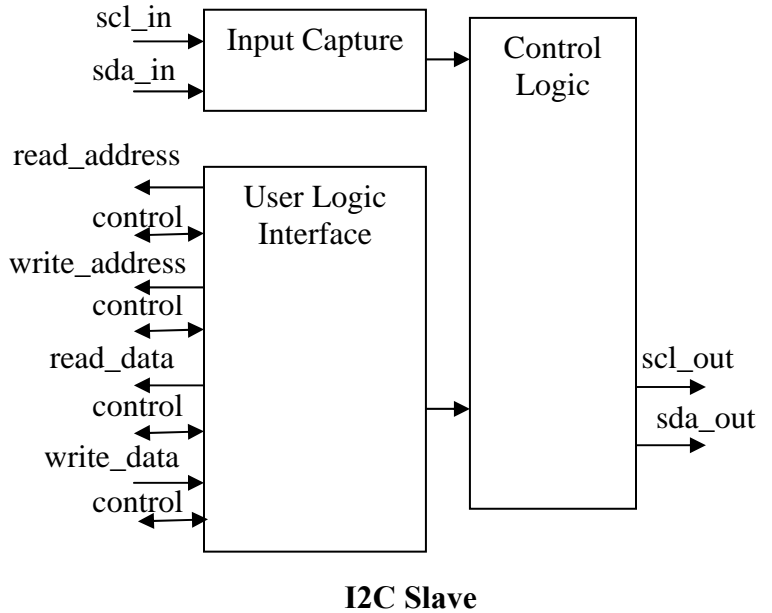
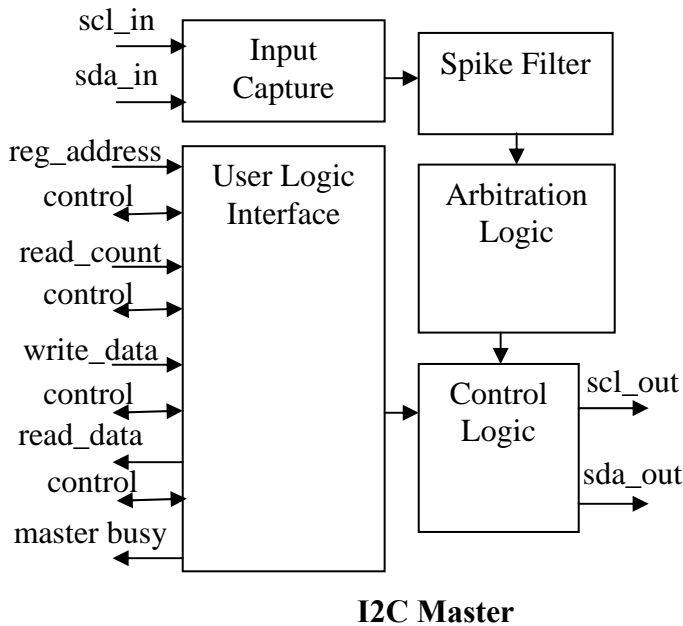
Introduction

For systems that have control functions that do not require high speed data transfer and/or where minimizing cost and interconnect wiring is desired, I2C serial bus is a popular choice.

These I2C interface modules implement spike suppression required for the Fast I2C protocol.

The user interface consists of 8-bit read and write busses, write enables and acknowledges.

This IP uses the I2C request/response protocol and assumes that a 1-byte command is used within a slave. This permits up to 256 1-byte registers or a 256x8 RAM or ROM to be implemented.



Implementation Summary

Core Specifics		
*Stratix IV EP4SGX (<i>example</i>)		
Speed Grade		
C8 or faster		
Resource Utilization		
	Master	
	<i>Typical</i>	
ALUTs	232	
Registers	210	
RAM	0	
	Slave	
	<i>Typical</i>	
ALUTs	135	
Registers	87	
RAM	0	
Supported Design Tools		
Altera	Quartus II 9.0 or later	

* Suitable for use in any Altera device family

Customization

The IP can be modified for a two-byte command if a larger address space is required. Please contact us to discuss your specific needs.

Deliverables

- VHDL or Verilog source code or encrypted source code depending upon license.

Product code: OCT-I2C-MASTER

OR

Product code: OCT-I2C-SLAVE
