

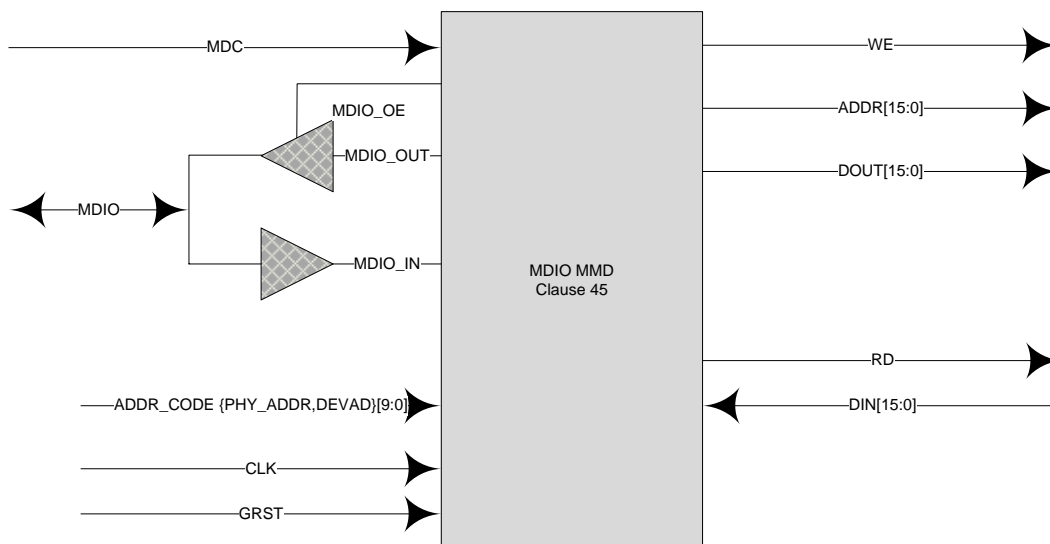
### Introduction

IEEE Standard 802.3 specifies a management data interface in Clause 22 and an extension in Clause 45 for the ability to access more device registers. This IP implements Clause 45 for an MDIO Manageable Device (MMD).

This IP has a small area footprint, and is simple to integrate.

### Features

- Implements Clause 45 of 802.3 Specification
- Phy address and DEVAD controlled by input ports
- MDIO inputs over-sampled for improved reliability
- Supports MDC clock speed up to 6Mhz
- IP runs from a system clock input of 100Mhz minimum, 125Mhz optimal
- Core interface to 16-bit wide 64K deep simple memory interface



### Implementation Summary

<b>Core Specifics</b>		
Cyclone 2, III, IV, and others		
<b>Speed Grade</b>		
All		
<b>Resource Utilization</b>		
	<i>Typical (Cyclone III)</i>	
LEs	206	
Registers	157	
RAM	0	
<b>Supported Design Tools</b>		
Altera	Quartus II 9.1SP2 or later	

### Deliverables

- Encrypted source code
- Optional Scripted verification environment with MDIO master BFM

**Product code: OCT-MDIO45**