

Introduction

A SD Host Controller conforms to the SD Host Controller Specification including the register set listed in the specification. This conformance allows a common SD driver firmware to operate with any specification-compliant SD Host Controller.

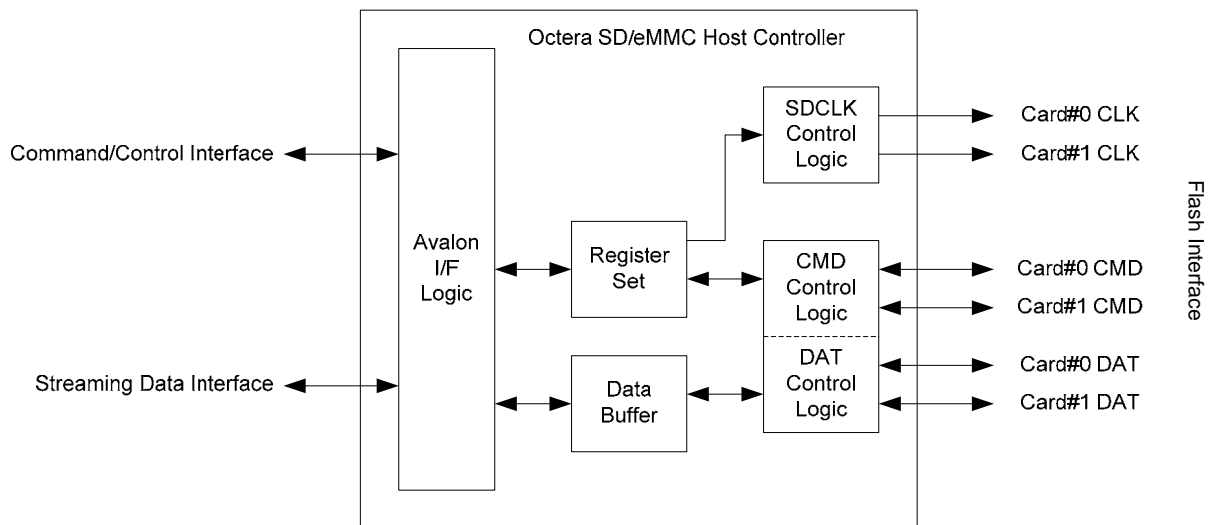
Embedded applications generally don't require all the features of a standard SD Host Controller such as hot-plug detection, scatter-gather DMA and security. Octera's SD/eMMC Host Controller is designed for these embedded uses using minimal hardware resources.

Octera's simplified SD/eMMC controller interface supports standard single SD/eMMC card operation as well as non-standard simultaneous streaming

data to and from two cards. The majority of the SD/eMMC protocol is implemented in firmware to reduce the hardware requirements.

Features

- Minimal hardware requirements.
- Maintain maximum data bandwidth during multiple block read and write operations.
- Support single as well as dual SD cards operating in parallel.
- Supports both SD1 (1-bit) and SD4 (4-bit) data bus configurations.
- SD/eMMC card clock rate at half the system clock rate (nominally 33 MHz).
- Operates on a single system clock.



Implementation Summary

Core Specifics		
Cyclone 3C5 and larger devices		
Speed Grade		
C8 or faster		
Resource Utilization		
	<i>Typical</i>	
LEs	759	
Registers	358	
RAM	0	
Supported Design Tools		
Altera	Quartus II 9.0 or later	

Deliverables

- Encrypted source code
- Scripted verification environment
- SD/MMC Bus Functional Models

Product code: OCT-SD/eMMC
